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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,847	09/12/2003	Shivraj G. Dharne	SC13027TC	7053

23125 7590 02/09/2005

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,847	DHARNE ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☒ Claim(s) *7-11* is/are allowed.

6)☒ Claim(s) *1,2,6,12 and 16-18* is/are rejected.

7)☒ Claim(s) *3-5,14,15,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities: Claim 14 incorrectly depends from newly canceled claim 13. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Runas (U.S. Patent No. 5,455,526).

In reference to claim 1, Runas discloses in Figure 1 an integrated circuit (100) with a bi-directional level shifter (101), the bi-directional level shifter comprising: a first signal terminal operable as an input and an output, wherein when being operable as an input, the first signal terminal receives a first signal compatible with a first voltage domain (3V) of the integrated circuit and wherein when being operable as an output, the first signal terminal provides a shifted signal compatible with the first voltage domain of the integrated circuit; a second signal terminal operable as an input and an output, wherein when being operable as an output, the second signal terminal provides a shifted signal compatible with a second voltage domain of the integrated circuit and wherein when being operable as an input, the second signal terminal receives a second signal compatible with the second voltage (5V) domain of the integrated circuit; and bi-

directional level shift circuitry (101) coupled between the first signal terminal and the second signal terminal, the bi-directional level shift circuitry translating the first signal compatible with the first voltage domain (3V) to the shifted signal compatible with the second voltage domain (5V) when the first signal terminal is operable as an input, the level shift circuitry (101) translating the second signal compatible with the second voltage domain (5V) to the shifted signal compatible with the first voltage domain (3V) when the second signal terminal is operable as an input (see column 4, lines 5-22). The same applies to claim 12 wherein the method includes cutting off current of a current path of the level shifter (101) between a first voltage domain voltage supply (3V) and a second voltage domain voltage supply (5V) when the voltage at the first signal terminal is at a high voltage.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Pinas et al. (U.S. Patent No. 6,507,506).

In reference to claim 1, Pinas discloses in Figure 2 an integrated circuit with a bi-directional level shifter (20), the bi-directional level shifter comprising: a first signal terminal operable as an input and an output, wherein when being operable as an input, the first signal terminal receives a first signal compatible with a first voltage domain (B36) of the integrated circuit and wherein when being operable as an output, the first signal terminal provides a shifted signal compatible with the first voltage domain of the

integrated circuit; a second signal terminal operable as an input and an output, wherein when being operable as an output, the second signal terminal provides a shifted signal compatible with a second voltage domain of the integrated circuit and wherein when being operable as an input, the second signal terminal receives a second signal compatible with the second voltage (B12) domain of the integrated circuit; and bi-directional level shift circuitry (20) coupled between the first signal terminal and the second signal terminal, the bi-directional level shift circuitry translating the first signal compatible with the first voltage domain (B36) to the shifted signal compatible with the second voltage domain (B12) when the first signal terminal is operable as an input, the level shift circuitry (20) translating the second signal compatible with the second voltage domain (B12) to the shifted signal compatible with the first voltage domain (B36) when the second signal terminal is operable as an input (see column 4, lines 12-30). The same applies to claim 12 wherein the method includes cutting off current of a current path of the level shifter (20) between a first voltage domain voltage supply (B36) and a second voltage domain voltage supply (B12) when the voltage at the first signal terminal is at a high voltage.

5. Claims 1, 2, 6, 12, and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (JP02003188710A).

In reference to claim 1, Watanabe discloses in Figure 4 an integrated circuit with a bi-directional level shifter, the bi-directional level shifter comprising: a first signal terminal operable as an input and an output, wherein when being operable as an input, the first signal terminal receives a first signal compatible with a first voltage domain (V_A)

of the integrated circuit and wherein when being operable as an output, the first signal terminal provides a shifted signal compatible with the first voltage domain of the integrated circuit; a second signal terminal operable as an input and an output, wherein when being operable as an output, the second signal terminal provides a shifted signal compatible with a second voltage domain of the integrated circuit and wherein when being operable as an input, the second signal terminal receives a second signal compatible with the second voltage (V_B) domain of the integrated circuit; and bi-directional level shift circuitry (102) coupled between the first signal terminal and the second signal terminal, the bi-directional level shift circuitry translating the first signal compatible with the first voltage domain (V_A) to the shifted signal compatible with the second voltage domain (V_B) when the first signal terminal is operable as an input, the level shift circuitry (102) translating the second signal compatible with the second voltage domain (V_B) to the shifted signal compatible with the first voltage domain (V_A) when the second signal terminal is operable as an input (see ABSTRACT). The same applies to claims 16 and 12 wherein the method includes cutting off current of a current path of the level shifter (102) between a first voltage domain voltage supply (V_A) and a second voltage domain voltage supply (V_B) when the voltage at the first signal terminal is at a high voltage. The same also applies to claim 2 and 17-18 wherein the level shift circuitry (102) further includes at least one cut-off transistor (102), wherein responsive to being non conductive, the at least one current cut-off transistor (102) operates to cut off current flowing in a current path between a first voltage domain voltage supply (V_A) and second voltage domain voltage supply (V_B) and the transistor (102) is an NFET.

In reference to claim 6, Watanabe discloses in Figure 4 wherein the level shifter has only signal lines that cross a domain boundary between the first voltage domain (V_A) and the second voltage domain (V_B).

Allowable Subject Matter

6. Claims 7-11 are allowed.

7. Claims 3-5, 14-15, and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claims 3-5 and 14 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein the level shift circuitry further comprises: a first transistor (425) located in the first voltage domain and a second transistor (426) located in the second voltage domain in combination with the rest of the limitations of the base claims and any intervening claims. Claim 15 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the circuit further comprises enabling circuitry (331) of a first circuit in combination with the rest of the limitations of the base claims and any intervening claims. Claims 19-20 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein the circuit includes a bias circuit (529) coupled to the gate of a first transistor (525) in combination with the rest of the limitations of the base claims and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: Claims 7-9 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry comprises: a current path between the first signal terminal (ST1) and the second signal terminal (ST2), the current path including a first transistor (325) and a second transistor (327), the first transistor (325) being disposed within the first voltage domain and having a first current terminal coupled to the first signal terminal (ST1), a control terminal coupled to a first voltage domain voltage supply (V_{DD1}), and a second current terminal, and the second transistor (327) being disposed within the second voltage domain and having a first current terminal coupled to the second signal terminal (ST2), a control terminal coupled to a second voltage domain voltage supply (V_{DD2}), and a second current terminal coupled to the second current terminal of the first transistor (325) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 10 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the level shift circuitry further comprises: a first transistor (323) located in the first voltage domain and having a first current terminal coupled to a first voltage domain voltage supply and a second current terminal coupled to the first signal terminal; a second transistor (321) located in the first voltage domain and having a first current terminal coupled the first voltage domain voltage supply, a second current terminal coupled to the control terminal of the first transistor, and a control terminal coupled to the first signal terminal; a third transistor (311) located in the second voltage domain and having a first current terminal coupled to a second voltage domain voltage supply and a second

current terminal coupled to the second signal terminal; a fourth transistor (313) located in the second voltage domain and having a first current terminal coupled the second voltage domain voltage supply, a second current terminal coupled to the control terminal of the third transistor, and a control terminal coupled to the second signal terminal in combination with the rest of the limitations of the base claims and any intervening claims. Claim 11 is allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the circuit further comprises a first circuit (331) including circuitry to enable the first circuit to receive the shifted signal from the first signal terminal and circuitry to enable the first circuit to provide the first signal and a second circuit (341) including circuitry to enable the second circuit to receive the shifted signal from the second signal terminal and circuitry to enable the second circuit to provide the second signal in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

February 4, 2005

TIMOTHY P. CALLAHAN
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